

UNITED STATES PATENT APPLICATION

FOR

**LEADFRAME PACKAGE WITH DUMMY CHIP**

Inventors: Johnson C. H. Tzu; Jerry Y. J. Wu; and Jung Yu Lee

Prepared By:  
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN  
12400 Wilshire Boulevard  
Seventh Floor  
Los Angeles, California 90025-1026  
(425) 827-8600

"Express Mail" mailing label number: EL431686267US

Date of Deposit April 9, 2001

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Sharon E. Farnus  
(Typed or printed name of person mailing paper or fee)

Sharon Farnus 4/9/01  
(Signature of person mailing paper or fee) (Date signed)

LEADFRAME PACKAGE WITH DUMMY CHIP

Field of the Invention

The present invention relates to a semiconductor  
5 package, and more specifically, to a lead frame  
package with a dummy chip.

Background of the Invention

Integrated circuits industry and fabrication  
10 involve the formation of semiconductor wafers,  
integrated circuits and chip package. With the advent  
of Ultra Large Scale Integrated (ULSI) circuits  
technologies, it has been a trend to scale down the  
geometry dimension of semiconductor devices and  
15 increase the density of semiconductor devices per  
unit area of silicon wafer. Thus, the sizes of devices  
have gotten smaller and smaller such that the area  
available for a single device has become very small.  
Further, the manufacturers of the devices are  
20 striving to reduce the sizes while simultaneously  
increasing their speed. Developments in interconnect  
and packing have been quite modest in comparison. The  
renewed interest in high density hybrid is driven by  
the requirement to handle large numbers of IC  
25 interconnections, the increasing clock rate of

digital systems and the desire to pack greater functionality into smaller spaces. Therefore, the number of a package's leads becomes more and more.

5        Therefore, an important consideration in making small, high speed and high-density devices is providing packages capable of the spreading heat generated by the devices. A further problem confronting the technology is the relentless need for  
10 more I/O per chip. Those issues lead to the requirement of more power for devices and the reduction of impedance of inductance. A conventional lead frame package with die paddle to receive the die does not have good performance in removing the heat  
15 generated by the devices, and it also has a limitation to increase the number of the package's leads. What is need is to provide a novel lead frame structure.

United States Patent No. 5,789,816 disclosed a  
20 lead frame structure, entitled "Multiple-chip integrated circuit package including a dummy chip". The inventor is Mr. Wu and assigned to assignee: United Microelectronics Corporation. The multiple-chip IC package is used to contain a number  
25 of chips therein. The multiple-chip IC package

includes a leadframe, at least one IC chip mounted on the first area of the leadframe, and at least one dummy chip is mounted on the second area of the leadframe. On the dummy chip, there is provided with a plurality of bonding pads which serve as intermediate bonding pads between the chips and the pins on the lead frame so that any two connecting points are connected by a number of straight wires via the dummy chip. This allows the wire bonding process to be much easier to conduct.

#### Summary of the Invention

The object of the present invention is to provide a lead frame package with a dummy package.

The lead frame package with dummy chip comprising a lead frame with a plurality of first leads, molding compound, a dummy chip and a die. Wherein the molding compound encapsulates the die and the dummy chip, the dummy chip is arranged on a lower portion of the molding compound. The die is stacked on an upper surface of the dummy chip by using an adhesive material. A plurality of bonding wires are connected between the die and an end of the plurality of leads over the dummy chip.

The dummy chip is formed of silicon and refers to a substrate without IC formed therein.

5                    Brief Description of the Drawings

FIGURE 1 is the cross section view of a structure according to the present invention.

~~FIGURE 2 is the top view of a structure of the first embodiment according to the present invention.~~

10            ~~FIGURE 3 is the top view of a structure of the first embodiment according to the present invention.~~

Detailed Description of the Preferred Embodiment

~~The present invention discloses a novel~~  
15            structure of a package 100. FIGURE 1 is a cross section view of an embodiment of the present invention and FIGURE 2 and FIGURE 3 are the top view of the present invention.

20            ~~As shown therein, the package 100 includes a lead~~  
frame 10 without conventional die paddle to receive the die. The lead frame 10 has inner leads 12 and outer leads 14. In the present invention, molding material (compound) 16 encapsulates a die 20 and a dummy chip  
25            18 configured as stacked structure. The dummy chip 18

24  
Cont.

is arranged on the lower portion of the molding compound 16 and the lower surface of the dummy chip 18 may be exposed. The dummy chip refers to the substrate without IC formed therein. Preferably, the material for the dummy chip 18 includes but not limited to silicon. The dummy chip 18 is fixed by the tapes 28 adhesive on the inner leads 12 of the lead frame 10. The die 20 is stacked on the upper surface of the dummy chip 18 by using adhesive material 26. The benefit of the present invention is that the metal sink is omitted, which may reduce the manufacture cost. Further, die paddle is not necessary for the present invention. The dummy chip 18 is exposed by the molding compound, which can improve the efficiency of spreading heat. General speaking, the die 20 generates a lot of heat during operation. The dummy chip 18 promotes thermal generated by the die 20 away from the die 20.

20 A plurality of bonding wires 24 are electrically connected between the die and the inner leads 12. The bonding wires 24 are used to provide electrical conductive path for signal transfer. The bonding wires 24 can be selected from gold, copper or  
25 conductive metal or alloy.

[illegible]

As is understood by a person skilled in the art, the foregoing preferred embodiments of the present invention are illustrated of the present invention rather than limiting of the present invention. It is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structure. Thus, while the preferred embodiment of the invention has been illustrated and described, it

